

ScanDIMM-168/NC

ScanDIMM-168/NC Boundary-Scan Based Digital Tester

User's Manual



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Chapter 1 Product Overview

Introduction

The ScanDIMM-168/NC Digital Tester module provides an easy-to-use method for interconnect testing of 168-pin Dual Inline Memory Module (DIMM) sockets. Through the use of Boundary-Scan technology, the ScanDIMM-168/NC Digital Tester provides 158 fully bi-directional test signals. A Boundary-Scan Test Access Port (TAP) connects to a host computer, which provides virtually unlimited memory depth for testing each of the DIMM socket pins. The 168-pin sockets are often used for Synchronous Dynamic Random Access Memory (SDRAM) memory modules, and the ScanDIMM-168/NC offers an accurate and easy-to-use mechanical and electrical solution for connecting test equipment to DIMM sockets.

Features of the ScanDIMM-168/NC

- Tests 168-pin DIMM sockets
- Tests for opens on the socket's power and ground pins
- 3.3V interface, 5V tolerant
- Daisy-chain an unlimited number of ScanDIMM-168/NC modules
- LED indicates power-on
- Compatible with ScanPlus software.

Figure 1-1 shows the ScanDIMM-168 module. (The NC version looks similar).

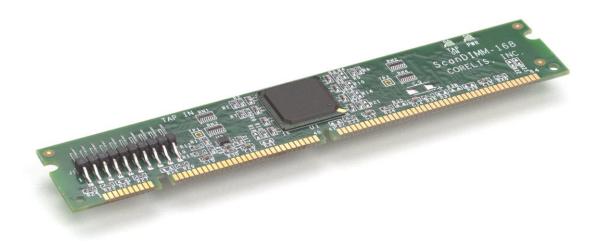


Figure 1-1. ScanDIMM-168 module (top view)

Product Overview

ScanDIMM-168/1.8V

The ScanDIMM-168/NC is designed to fit into the popular 168-pin, 3.3V-compatible DIMM socket. A similar module, the ScanDIMM-168/NC/1.8V, fits into a 1.8V-compatible DIMM socket. This manual applies to both the 3.3V and 1.8V modules but for the sake of simplicity it references only the more popular 3.3V module. For ordering information on the 1.8V version, please contact sales@corelis.com.

Daisy-Chaining the TAPs

Multiple ScanDIMM-168/NCs give access to units under test (UUTs) that contain multiple DIMM sockets. Simply connect the TDO from one socket to the TDI on the next.

ScanDIMM-168/NC Specifications

Size and Form Factor

Compatibility JEDEC MO-161

Dimensions 5.250 in. × 1.000 in. (JEDEC MO-161 AA

dimension)

PCB thickness 0.050 inches

Connector Keying 3.3V-compatible, 1.8V version also available

Number of Boundary-Scan Test Signals

158 per module

Maximum Test Clock (TCK) Frequency

Maximum TCK Frequency 25 MHz

LEDs

PWR Indicates 3.3V power source is present

I/O and TAP Signals DC Characteristics

Parameter	ameter Conditions		MAX	UNIT
Operating Power (V_{DD}) – Provided via the 168 pin socket pins		3.00	3.60	V
High Level Input Voltage (V_{IH})		2.0	5.5	V
Low Level Input Voltage (V_{II})		-0.30	0.80	V
Output High Lovel Waltage (V.)	I _{OH} = -4 mA dc	2.90		V
Output High Level Voltage (V_{OH})	I _{OH} = -0.1 mA dc	3.10		V
Outroot I and I and Walter of W.	I_{OL} = 8 mA dc		0.40	V
Output Low Level Voltage (V _{OL})	$I_{\rm OL}$ = 0.1 mA dc		0.20	V
Input leakage Current (I _I)	$V_I = V_{DD}$ or GND		10	μА

Table 1-1. DC Characteristics

Power Requirements (Provided by the 168-pin mating socket)

3.30 V 0.200 A (Maximum)

Operating Environment

Temperature 0°C to 55°C

Relative Humidity 10% to 90%, non-condensing

Storage Environment

Temperature -40°C to 85°C

Chapter 2 ScanDIMM-168/NC Installation

The ScanDIMM-168/NC product consists of the following components:

- ScanDIMM-168/NC Module
- User's Manual
- Configuration Disk

Ensure all materials listed are present and free from visible damage or defects before proceeding. If anything appears to be missing or damaged, please contact Corelis at the number listed on the title page.

What's on the Disk

The disk contains the ScanDIMM-168/NC BSDL file:

Filename	Description		
ScanDIMM-168NC.bsd	BSDL file for the ScanDIMM-168/NC Boundary-Scan component.		

Unit Under Test Board Layout

The Unit Under Test must be designed to support the ScanDIMM-168/NC module. The TAP signals of the ScanDIMM-168/NC are connected to the edge connector that plugs into the socket on the unit under test as shown in Table 2-1.

DIMM Pin	Signal Name	I/O	Description
44	TDI	In	Test Data In (to UUT)
48	TDO	Out	Test Data Out (from UUT)
80	TMS	In	Test Mode Select
81	TCK	In	Test Clock

Table 2-1. TAP Connection List

The TDI to the socket should come from the TDO of a component in the scan chain or from the connector. The TDO from the socket should go to the next component in the scan chain or to the connector. The TMS and TCK from the Unit Under Test TAP must be connected to the socket as well as any other boundary-scan components. Treat all TAP signals, especially TMS and TCK, as critical nets. It is recommended that pull-up and pull-down resistors be placed at the end of the TCK clock trace.

Daisy-Chaining Multiple ScanDIMM-168/NC Modules

To daisy-chain multiple ScanDIMM-168/NC modules, simply connect the TDO of one module to the TDI of the next. TMS and TCK should be brought to all modules.

Indicator LED

The LED indicates the status of the ScanDIMM-168/NC module. D2 is labeled PWR. It illuminates if the ScanDIMM-168/NC is receiving power from the target (through pins 41 and 84). If the LED is not illuminated, the ScanDIMM-168/NC module is not powered up.

Chapter 3

Preparation of Test Input Files

Introduction

The ScanDIMM-168/NC integrates easily with a boundary-scan test plan. When the ScanDIMM-168/NC is installed in a socket, the socket behaves like a boundary-scan component. Therefore, it is not necessary to make any changes to the netlist to include the ScanDIMM-168/NC in a test plan.

Once the ScanDIMM-168/NC is plugged into the socket on the target board, the boundary-scan test system will automatically test the socket. However, regeneration of the interconnect tests with the included ScanDIMM-168/NC BSDL file is required (using ScanExpressTPG).

Copy the file **ScanDIMM-168NC.bsd** to your design directory.

Proceed through the ScanExpressTPG test generation steps normally until you get to the BSDL files screen shown in Figure 3-1. This screen is used to detect the scan chain ordering and provide information about the physical characteristics of the JTAG compatible devices on the board.

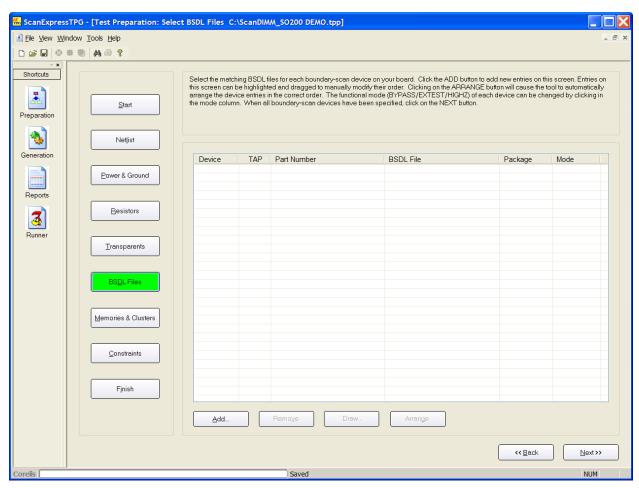


Figure 3-1. ScanExpressTPG BSDL Files Phase

Click on the Add button and the "Add BSDL Files" window will appear as shown in Figure 3-2. This screen shows the most likely devices to be boundary scan compatible on the left and all BSDL files in the project directory on the right.

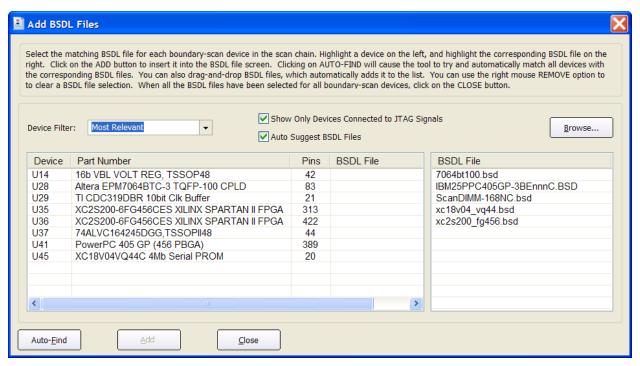


Figure 3-2. ScanExpressTPG Add BSDL Files Screen

Click the Auto-Eind button to cause ScanExpressTPG to try to make a best guess as to which devices are boundary scan components and which BSDL files they should be associated with. A popup similar to Figure 3-3 will appear to indicate how many devices were found.



Figure 3-3. ScanExpressTPG Added New Devices

Click on the OK button to close the popup. Devices which have been assigned a BSDL file are colored in blue.

Change the device filter option to *All Devices* to allow the ScanDIMM-168/NC device to be seen. Figure 3-4 below shows an example target system with an Altera CPLD and a ScanDIMM-168/NC module associated with their BSDL files.

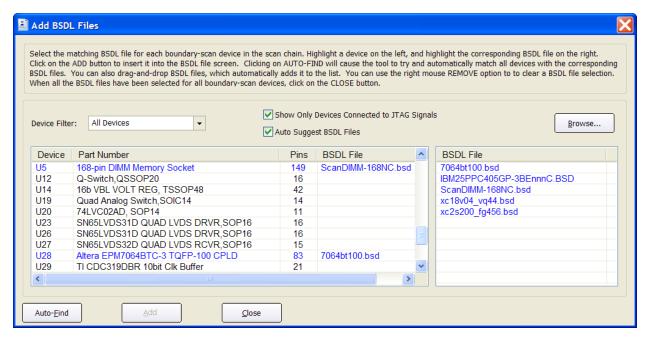


Figure 3-4. ScanExpressTPG Add BSDL Files Screen After Auto-Find

Click on the *Close* button to return to the BSDL files screen.

The BSDL files screen now contains entries for all JTAG compatible devices on the board. An example is shown in Figure 3-5.

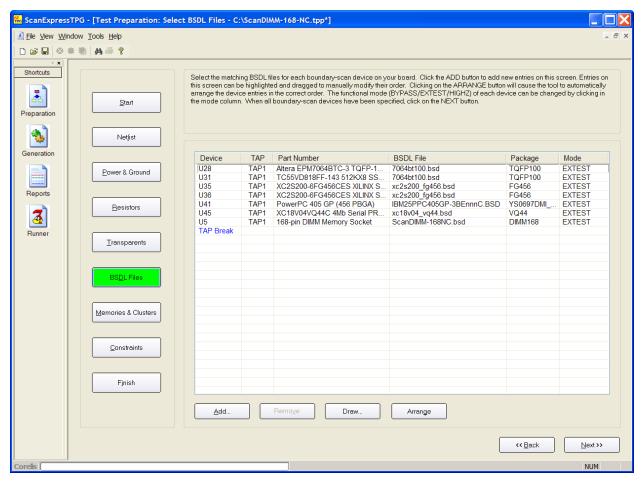


Figure 3-5. ScanExpressTPG Populated BSDL Files Screen

The JTAG devices must appear on this screen in the actual order that they are in the scan chain on the board. Select the ScanDIMM entry and right-click to bring up the menu. Select *Move Down* as shown in Figure 3-6 to move the ScanDIMM entry down the list until it is at the bottom.

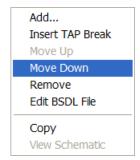


Figure 3-6. ScanExpressTPG Move Down Menu Selection

Click on the Arrange button and ScanExpressTPG will attempt to put the devices into the correct order. The status window shown will appear to show the processing status. The warnings about the netlist not having a connection to the ScanDIMM may be safely ignored.

This window also displays any detected compliance enable information. Compliance enable conditions must be met for the JTAG devices to function properly. When the processing completes, click on the OK button to close the status window.

The BSDL files screen now contains entries for all JTAG compatible devices on the board in the correct order with associated TAP Breaks. This can be seen in Figure 3-7.

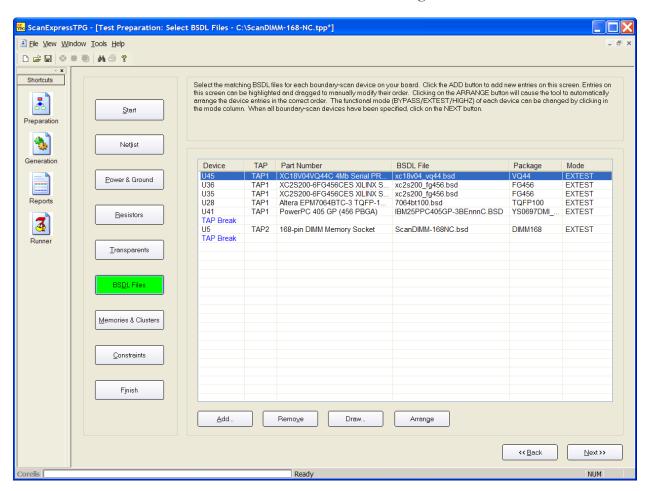


Figure 3-7. ScanExpressTPG BSDL File Phase with TAP Break

Click the *Next* button to proceed with the rest of the test generation steps. ScanExpressTPG will use the input files to generate the actual test patterns that will be applied to the board by ScanPlus Runner.

Testing the Socket Power and Ground Pins

To test the power and ground pins on the ScanDIMM-168/NC socket, the constraint file should have added syntax:

SENSE_HIGH **VDD** SENSE_LOW **GND**

Where **VDD** and **GND** are the net names of the 3.3V SDRAM power and ground signals on the target board. This syntax may already be present to test other power or ground connections in the target system.